CLAIMS

An output stage for providing a substantially symmetrical rail-to-rail output

1.

1

1

2

6.

8 V _{EE} and wherein the second drain is coupled to the first drain; and 9 an output sink network coupled to the second gate, wherein the output sink network drives the second field effect device such that a product of a first current in the first field effect device and a second current in the second field effect device is substantially equal to predetermined constant. 2. An output stage as recited in claim 1, wherein a sum of the first current and the second current is essentially equal to a predetermined constant during operation of the output stage. 3. An output stage as recited in claim 1, wherein the first field effect device is configured in a common source configuration. 4. An output stage as recited in claim 1, wherein the first field effect device is P-channel metal oxide semiconductor field effect (PMOS) transistor. 5. An output stage as recited in claim 4, wherein the second field effect device	2	voltage, the output stage comprising:		
a second field effect device complementary to the first field effect device, wherein second field effect device includes a second source, second drain, and second gate, and wherein the second source is coupled to a power supply having a nominal voltage supply of Vee and wherein the second drain is coupled to the first drain; and 9 an output sink network coupled to the second gate, wherein the output sink network drives the second field effect device such that a product of a first current in the first field effect device and a second current in the second field effect device is substantially equal to predetermined constant. 1 2. An output stage as recited in claim 1, wherein a sum of the first current and the second current is essentially equal to a predetermined constant during operation of the output stage. 3. An output stage as recited in claim 1, wherein the first field effect device is configured in a common source configuration. 4. An output stage as recited in claim 1, wherein the first field effect device is P-channel metal oxide semiconductor field effect (PMOS) transistor.	3	a firs	t field effect device having a first source, first drain, and first gate, the first	
second field effect device includes a second source, second drain, and second gate, and wherein the second source is coupled to a power supply having a nominal voltage supply of Vee and wherein the second drain is coupled to the first drain; and an output sink network coupled to the second gate, wherein the output sink network drives the second field effect device such that a product of a first current in the first field effect device and a second current in the second field effect device is substantially equal to predetermined constant. 2. An output stage as recited in claim 1, wherein a sum of the first current and the second current is essentially equal to a predetermined constant during operation of the output stage. 3. An output stage as recited in claim 1, wherein the first field effect device is configured in a common source configuration. 4. An output stage as recited in claim 1, wherein the first field effect device is P-channel metal oxide semiconductor field effect (PMOS) transistor.	4	source being	coupled to a power supply V _{CC} ;	
wherein the second source is coupled to a power supply having a nominal voltage supply of Vee and wherein the second drain is coupled to the first drain; and an output sink network coupled to the second gate, wherein the output sink network drives the second field effect device such that a product of a first current in the first field effect device and a second current in the second field effect device is substantially equal to predetermined constant. 2. An output stage as recited in claim 1, wherein a sum of the first current and the second current is essentially equal to a predetermined constant during operation of the output stage. 3. An output stage as recited in claim 1, wherein the first field effect device is configured in a common source configuration. 4. An output stage as recited in claim 1, wherein the first field effect device is P-channel metal oxide semiconductor field effect (PMOS) transistor.	5	a sec	ond field effect device complementary to the first field effect device, wherein the	
8 V _{EE} and wherein the second drain is coupled to the first drain; and 9 an output sink network coupled to the second gate, wherein the output sink network drives the second field effect device such that a product of a first current in the first field effect device and a second current in the second field effect device is substantially equal to predetermined constant. 2. An output stage as recited in claim 1, wherein a sum of the first current and the second current is essentially equal to a predetermined constant during operation of the output stage. 3. An output stage as recited in claim 1, wherein the first field effect device is configured in a common source configuration. 4. An output stage as recited in claim 1, wherein the first field effect device is P-channel metal oxide semiconductor field effect (PMOS) transistor. 5. An output stage as recited in claim 4, wherein the second field effect device	- 6	second field effect device includes a second source, second drain, and second gate, and		
an output sink network coupled to the second gate, wherein the output sink network drives the second field effect device such that a product of a first current in the first field effect device and a second current in the second field effect device is substantially equal to predetermined constant. 2. An output stage as recited in claim 1, wherein a sum of the first current and the second current is essentially equal to a predetermined constant during operation of the output stage. 3. An output stage as recited in claim 1, wherein the first field effect device is configured in a common source configuration. 4. An output stage as recited in claim 1, wherein the first field effect device is P-channel metal oxide semiconductor field effect (PMOS) transistor.	7	wherein the second source is coupled to a power supply having a nominal voltage supply of		
drives the second field effect device such that a product of a first current in the first field effect device and a second current in the second field effect device is substantially equal to predetermined constant. 2. An output stage as recited in claim 1, wherein a sum of the first current and the second current is essentially equal to a predetermined constant during operation of the output stage. 3. An output stage as recited in claim 1, wherein the first field effect device is configured in a common source configuration. 4. An output stage as recited in claim 1, wherein the first field effect device is P-channel metal oxide semiconductor field effect (PMOS) transistor. 5. An output stage as recited in claim 4, wherein the second field effect device	8	V_{EE} and wherein the second drain is coupled to the first drain; and		
output stage. 3 output stage as recited in claim 1, wherein the first field effect device is configured in a common source configuration. 4. An output stage as recited in claim 1, wherein the first field effect device is P-channel metal oxide semiconductor field effect (PMOS) transistor. 5. An output stage as recited in claim 4, wherein the second field effect device	_	an output sink network coupled to the second gate, wherein the output sink network		
output stage. 3 output stage as recited in claim 1, wherein the first field effect device is configured in a common source configuration. 4. An output stage as recited in claim 1, wherein the first field effect device is P-channel metal oxide semiconductor field effect (PMOS) transistor. 5. An output stage as recited in claim 4, wherein the second field effect device	10	drives the second field effect device such that a product of a first current in the first field		
output stage. 3 output stage as recited in claim 1, wherein the first field effect device is configured in a common source configuration. 4. An output stage as recited in claim 1, wherein the first field effect device is P-channel metal oxide semiconductor field effect (PMOS) transistor. 5. An output stage as recited in claim 4, wherein the second field effect device	11	effect device and a second current in the second field effect device is substantially equal to a		
output stage. 3 output stage as recited in claim 1, wherein the first field effect device is configured in a common source configuration. 4. An output stage as recited in claim 1, wherein the first field effect device is P-channel metal oxide semiconductor field effect (PMOS) transistor. 5. An output stage as recited in claim 4, wherein the second field effect device	12	predetermined constant.		
output stage. 3 output stage as recited in claim 1, wherein the first field effect device is configured in a common source configuration. 4. An output stage as recited in claim 1, wherein the first field effect device is P-channel metal oxide semiconductor field effect (PMOS) transistor. 5. An output stage as recited in claim 4, wherein the second field effect device	H. H.			
output stage. 3 output stage as recited in claim 1, wherein the first field effect device is configured in a common source configuration. 4. An output stage as recited in claim 1, wherein the first field effect device is P-channel metal oxide semiconductor field effect (PMOS) transistor. 5. An output stage as recited in claim 4, wherein the second field effect device	1	2.	An output stage as recited in claim 1, wherein a sum of the first current and	
configured in a common source configuration. 4. An output stage as recited in claim 1, wherein the first field effect device is P-channel metal oxide semiconductor field effect (PMOS) transistor. 5. An output stage as recited in claim 4, wherein the second field effect device	<u>1</u> 2	the second current is essentially equal to a predetermined constant during operation of the		
configured in a common source configuration. 4. An output stage as recited in claim 1, wherein the first field effect device is P-channel metal oxide semiconductor field effect (PMOS) transistor. 5. An output stage as recited in claim 4, wherein the second field effect device	T. 3	output stage.		
configured in a common source configuration. 4. An output stage as recited in claim 1, wherein the first field effect device is P-channel metal oxide semiconductor field effect (PMOS) transistor. 5. An output stage as recited in claim 4, wherein the second field effect device	#5## ## ##	9		
configured in a common source configuration. 4. An output stage as recited in claim 1, wherein the first field effect device is P-channel metal oxide semiconductor field effect (PMOS) transistor. 5. An output stage as recited in claim 4, wherein the second field effect device		3.	An output stage as recited in claim 1, wherein the first field effect device is	
 P-channel metal oxide semiconductor field effect (PMOS) transistor. 5. An output stage as recited in claim 4, wherein the second field effect device 	* .			
 P-channel metal oxide semiconductor field effect (PMOS) transistor. 5. An output stage as recited in claim 4, wherein the second field effect device 	1	4.	An output stage as recited in claim 1, wherein the first field effect device is a	
To the second as the second and the second areas and the second areas are the second areas are second are second areas are second are second areas areas are second areas are second areas areas are second areas are second areas are second areas areas areas areas are second areas	2			
To the second as the second and the second areas and the second areas are the second areas are second are second areas are second are second areas areas are second areas are second areas areas are second areas are second areas are second areas areas areas areas are second areas	1	5.	An output stage as recited in claim 4, wherein the second field effect device is	
an in-challief fietal oxide semiconductor field effect (NMOS) transistor.	2	* ,	metal oxide semiconductor field effect (NMOS) transistor.	

a current mirror to track the current in the first field effect device.

An output stage as recited in claim 5, wherein the output sink network utilizes

- 7. An output stage as recited in claim 6, wherein the current mirror tracks the current in the first field effect device at a predetermined ratio of the current in the first field.
- 8. An output stage as recited in claim 1, wherein the first field effect device is an N-channel metal oxide semiconductor field effect (NMOS) transistor.
- 9. An output stage as recited in claim 8, wherein the second field effect device is a P-channel metal oxide semiconductor field effect (PMOS) transistor.
- 1 10. An output stage as recited in claim 1, wherein a substantially rail-to-rail output voltage produced by the output stage is no more than one V_{GS} and two V_{Dsat} from either rail.
 - 11. A method for providing an output signal from an output stage of a low voltage operation amplifier capable of providing a substantially rail-to-rail output voltage, the method comprising the operations of:
 - providing an input signal to a first field effect device having a first source, first drain, and first gate, the first source being coupled to a power supply $V_{\rm CC}$; and
 - driving a second complimentary field effect device utilizing an output sink network such that a product of a first current in the first field effect device and a second current in the second field effect device is substantially equal to a predetermined constant.
- 1 12. A method as recited in claim 11, wherein a sum of the first current and the 2 second current is essentially equal to a predetermined constant during operation of the 3 amplifier.
- 1 13. A method as recited in claim 11, wherein the first field effect device is 2 configured in a common source configuration.
- 1 14. A method as recited in claim 13, wherein the first field effect device is a Pchannel metal oxide semiconductor field effect (PMOS) transistor.

15.

1 2

1 2

12

1

2

16.	A method as recited in claim 15, further comprising the operation of tracking	
the current in the first field effect device utilizing a current mirror.		

N-channel metal oxide semiconductor field effect (NMOS) transistor.

A method as recited in claim 14, wherein the second field effect device is an

- 17. A method as recited in claim 16, wherein the current mirror tracks the current in the first field effect device at a predetermined ratio.
- 18. A method as recited in claim 11, further comprising the operation of producing an essentially rail-to-rail output voltage, the essentially rail-to-rail output voltage being no more than one V_{GS} and two V_{Dsat} from either rail.
 - 19. An application specific integrated circuit (ASIC) having an output stage for a low voltage operational amplifier, the ASIC comprising:
 - a first field effect device having a first source, first drain, and first gate, the first source being coupled to a power supply $V_{\rm CC}$;
 - a second field effect device complementary to the first field effect device, wherein the second field effect device includes a second source, second drain, and second gate, and wherein the second source is coupled to a power supply having a nominal voltage supply of V_{EE} and wherein the second drain is coupled to the first drain; and
- an output sink network coupled to the second gate, wherein the output sink network drives the second field effect device such that a product of a first current in the first field effect device and a second current in the second field effect device is essentially equal to a predetermined constant during operation of the output stage.
- 20. An ASIC as recited in claim 19, wherein the first field effect device is configured in a common source configuration.
- 1 21. An ASIC as recited in claim 19, wherein the first field effect device is a P-2 channel metal oxide semiconductor field effect (PMOS) transistor.

1

2

1

2

3

4

2

1 2

3 4

5

1 2

3

- 22. An ASIC as recited in claim 21, wherein the second field effect device is an 1 N-channel metal oxide semiconductor field effect (NMOS) transistor. 2
 - An ASIC as recited in claim 22, wherein the output sink network utilizes a 23. current mirror to track the current in the first field effect device.
 - An ASIC as recited in claim 23, wherein the current mirror tracks the current 24. in the first field effect device at a predetermined ratio. A method as recited in claim 13, wherein the current mirror tracks the current in the first field effect device at a predetermined ratio.
- 25. An ASIC as recited in claim 24, wherein the predetermined ratio is about 6:1. 1
 - 26. An ASIC as recited in claim 19, wherein a substantially rail-to-rail output voltage produced by the output stage is no more than one V_{GS} and two V_{Dsat} from either rail.
 - 27. An operational amplifier output stage suitable for low voltage operation and capable of providing a substantially rail-to-rail output voltage, the output stage comprising:
 - a push-pull output network, wherein the push-pull output network receives a first input signal and a second input signal, the first input signal being provided by an input signal V_{IN}; and
- an output sink network, wherein the output sink network provides the second input 6 7 signal to the push-pull output network.
 - 28. An operational amplifier output stage as recited in claim 27, wherein the pushpull output network includes a first field effect device and a second complimentary field effect device.
- 29. 1 An operational amplifier output stage as recited in claim 28, wherein the first field effect device is configured in a common source configuration. 2

1

2

5

6

1

2

3

4

1

- 1 30. An operational amplifier output stage as recited in claim 29, wherein the output sink network utilizes a current mirror to track the current in the first field effect device.
- 1 31. An operational amplifier output stage as recited in claim 30, wherein the current mirror tracks the current in the first field effect device at a predetermined ratio.
 - 32. An operational amplifier suitable for operating on low input voltages and capable of providing a substantially symmetrical rail-to-rail output voltage, the operational amplifier comprising:
- 4 an input stage; and
 - an output stage coupled to the input stage, wherein the output stage includes an output sink network.
 - 33. An operational amplifier as recited in claim 32, wherein the output stage further includes a push-pull output network, wherein the push-pull output network receives a first input signal and a second input signal, the first input signal being provided by an input signal $V_{\rm IN}$.
 - 34. An operational amplifier as recited in claim 33, wherein the output sink network provides the second input signal to the push-pull output network.